Government College of Engineering, Aurangabad
(An Autonomous Institute of Government of Maharashtra)

T.E. (CSE) Examination
End Semester Examination Nov 2016

CS 341: Computer Organization & Architecture

12 4 NOV 2016

Time: Three Hours *Max Marks: 60*

"Verify the Course Code and check whether you have got the correct question paper"

N.B:-
1. All questions are compulsory
2. Figures to the right indicate full marks
3. Assume suitable data if necessary and state it clearly
4. Use of non-programmable calculator is allowed

Q.1 Attempt all (12)

a) Explain the structure of a computer system.
b) Use the Booth algorithm to multiply 23 (multiplicand) by 29 (multiplier), where each number is represented using 6 bits.

Q. 2 Attempt any two (12)

a) A benchmark program is run on a 40 MHz processor. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count:

Instruction Type	Instruction Count	Cycles per Instruction
Integer arithmetic	45000	1
Data transfer	32000	2
Floating point	15000	2
Control transfer	8000	2

Determine the effective CPI, MIPS rate, and execution time for this program

b) Explain synchronous and asynchronous timing bus operation.
c) Find the following differences using twos complement arithmetic:
a. 111000-101011 **b.** 11001100- 101110 **c.** 111000001111-110011110011

Q.3 Attempt any two (12)

a) Explain different addressing mode with example.
b) A program p1 of 100 instructions is implemented with 5 stage instruction pipeline. Each stage is having uniform delay of 10ns. The program P2 of 2000 instructions is also implemented using the same pipeline
   1. Calculate the time required for both program.
   2. Compute the speed up factors for each case
   3. What will be the efficiencies extracted by the programs from the pipeline.
c) Explain Error correcting code with example.

Q.4 Attempt any two (12)

a) Explain different level of RAID.
b) Explain the specific features of all types of RAMs and ROMs.
c) It is required to implement 100 instruction program in a 4 stage pipeline such that stage 2 delay is twice the stage 1 delay and half of the stage 3 delay. The stage 4 and stage 2 delay are same. The stage 3 delay is 40ns. How much time is required to complete 100 and 1000 instructions? What is the speed up for both?

Q.5 Attempt the following (12)

a) What is the basic advantage of using interrupt initiated data transfer over transfer under program controlled without an interrupt?
b) Consider a scenario where you have a photo studio and you want to purchase a printer which can give you high efficiency and high quality graphics. You have three options dot matrix, desk jet and laser printer. Out of these which printer will you use and why. What will be the reasons for rejecting the other two?